

IN THE DRAWINGS

The attached sheets of drawings include changes to Figs. 9 and 10. These sheets, which include Figs. 9 and 10, replace the original sheets including Figs. 9 and 10.

Attachment: Replacement Sheets (2)

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-6 are pending in the present application. Claims 1-6 are amended and Claims 7-10 are added by the present amendment.

Amendments to Claims 1-6 and new Claims 7-10 find support in the specification and claims as originally filed, at least at Figure 3. Thus, no new matter is added.

In the outstanding Office Action, the drawings were objected to; Claim 4 was objected to; Claims 4-6 were rejected under 35 U.S.C. § 112, second paragraph; Claim 1 was rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,748,569 to Teodorescu et al. (herein “Teodorescu”); and Claims 2-6 were indicated as allowable if rewritten in independent form and to overcome the rejection under 35 U.S.C. 112, second paragraph.

Applicant gratefully acknowledges the Examiner’s indication of allowable subject matter. In light of this indication, original dependent Claim 2 is rewritten in independent form and new dependent Claims 7-10 corresponding to original Claims 3-6 are added to depend from amended Claim 2.

Accordingly, Applicant respectfully submits independent Claim 2 and claims depending therefrom are allowable.

Applicant and Applicant’s representatives thank the Examiner for the courtesy of a personal interview with Applicant’s representatives on October 5, 2005. During the interview, differences between the applied reference and Claim 1 of the invention were discussed. Comments discussed during the interview are reiterated below.

In response to the objection to the drawings, replacement sheets labeling Figures 9 and 10 as Background Art are submitted. Accordingly, the grounds for the objection are believed to be overcome.

In response to the objection to Claim 4 for informalities and the rejection to Claims 4-6 under 35 U.S.C. § 112, second paragraph, Claims 4-6 are amended in light of the comments noted in the outstanding Office Action. Accordingly, it is respectfully requested the objection and rejection be withdrawn.

Amended independent Claim 1 is directed to a clock generation circuit including, in part, at least one phase control circuit configured to match a phase of one output of the plurality of the former stage PLL circuits with another output of a former stage PLL circuit.

In a non-limiting example, Figure 3 shows a schematic view of a clock generation circuit. Reference signals (1a and 1b) are inputted into a plurality of former stage phase locked loop circuits (2a and 2b) that generate primary clocks. Phase control circuits (7a and 7b) receive at least one primary clock output of the plurality of former stage phase locked loop circuits (2a and 2b). The phase control circuit matches a phase of the primary clock received with another primary clock outputted from one of the plurality of former stage phase locked loop circuits (2a and 2b). A selection circuit (4), based upon selection signal (3), selects one of the phase matched primary clocks outputted from the phase control circuit and later stage phase locked loop circuit (5) then generates a clock signal (6) which is synchronized with the selected primary clock.

As discussed during the interview, Teodorescu does not disclose or suggest a phase control circuit that matches a phase of one output from a former stage PLL circuit to a phase of an output from another former stage PLL circuit. Teodorescu describes a fault detection system that allows switching circuitry to switch from a clock signal to a redundant clock signal when there is an error with the clock signal. As shown in Figure 1, timing subsystems (14 and 16) including phase locked loops (18 and 20) receive clock signal (10) and redundant clock signal (12), respectively.¹ In other words, clock signal (10) and redundant clock signal

¹ Teodorescu, column 3, lines 5-13.

(12) are copies of the same signal having a same phase. The phase locked loops (18 and 20) monitor the redundant signals (10 and 12) and generate loss of lock signals (26 and 28).² The loss of lock signal (26 or 28) will prevent the switching circuitry (34) from selecting a redundant signal (10 or 12) with any errors.³ For example, if loss of lock signal (26) indicates that redundant signal (10) has failed, switching circuitry (34) will select the other redundant signal (12). In other words, Teodorescu merely describes switching to a redundant copy of a clock signal when the clock signal fails. However, Teodorescu does not describe any phase control circuit matching phases of former stage PLL circuits because the clock signal and redundant clock signal of Teodorescu already have the same phase.

Accordingly, Applicant respectfully submits that Teodorescu does not disclose or suggest a clock generation circuit including “a plurality of phase control circuits each configured to match a phase of an output from a former stage PLL circuit in the plurality of former stage PLL circuits to a phase of an output from another former stage PLL, and generate a phase matched output,” as recited in amended Claim 1.

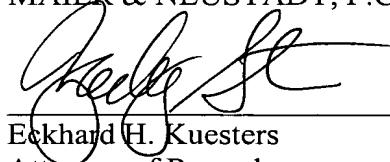
Accordingly, Applicant respectfully submits that independent Claim 1 and each of the claims depending therefrom are allowable.

² Teodorescu, column 3, lines 18-21.
³ Teodorescu, column 3, lines 40-48.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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